UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TSUKASA YAJIMA

Appeal No. 2005-0520
Application No. 09/768,271

ON BRIEF

Before KIMLIN, GARRIS and PAWLIKOWSKI, Administrative Patent Judges.

KIMLIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 6-9 and 11-19, all of the claims remaining in the present application.

Claim 6 is illustrative:

6. A semiconductor device comprising:

first and second gates formed on active regions of a substrate, said first and second gates each consisting of a refractory metal layer on a polysilicon layer;

a field oxide formed on the substrate between said first and second gates;

side walls formed on side surfaces of said first and second gates, said side walls being a silicon oxide film;

a protective layer formed selectively on said field oxide to prevent overetching of said field oxide, said protective layer being a material different than said field oxide; and

an insulating layer, a contact hole, and a connecting wire formed above a surface of the substrate.

The examiner relies upon the following reference in the rejection of the appealed claims:

Yoo et al. (Yoo)	5,605,853	Feb. 25, 1997

Appellant's claimed invention is directed to a semiconductor device comprising first and second gates, a field oxide formed on the substrate between the gates, and a protective layer of poly-silicon formed on the field oxide. According to appellant, "[p]olysilicon layer 12 prevents etching of field oxide 34 during this overetching of oxide layer 36, preventing decreases of field isolation voltage caused by thinning of field oxide 34 (page 14, lines 1-7)" (page 4 of Brief, second paragraph).

Appealed claims 6-9 and 11-19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yoo.

It is appellant's "wish to group all of claims 6-9 and 11-19 together." Accordingly, all of the appealed claims stand or fall together with claim 6.

We have throughly reviewed each of appellant's arguments for patentability, including the prior art evidence relied upon in support thereof. However, we are in complete agreement with the examiner that Yoo describes the claimed subject matter on appeal within the meaning of § 102. Accordingly, we will sustain the examiner's rejection for essentially those reasons expressed in the Answer, and we add the following primarily for emphasis.

Appellant does not dispute that the figures illustrated in the Yoo patent depict all of the features of the claimed semi-conductor device. It is appellant's contention that protective polysilicon floating gate 21 of Yoo, although shown in the reference drawings as on the field oxide, cannot, in fact, be formed on field oxide layer 12 and still function as a working floating gate. According to appellant, "a floating gate typically must be formed on a relatively thin insulating layer, such as a tunnel oxide layer, so that exchange of charges between the diffusion layer and the floating gate may occur" (page 6 of

Brief, first paragraph). Appellant cites three references in support of this proposition.[1] Appellant maintains that relatively thin gate oxides are formed under floating gates, and appellant submits that "it should be understood that floating gate electrodes in general are formed on relatively thin gate oxides, as opposed to relatively thick field oxide layers" (page 7 of Brief, first paragraph, emphasis added). Appellant reasons that "one of ordinary skill should understand that floating gate 21 in Figs. 2-7 of the Yoo et al. reference cannot be formed on FOX layer 12 and be a functional floating gate" (page 8 of Brief, second paragraph). Appellant then concludes that "[f]loating gate 21 of the Yoo et al. reference is not specifically described as formed on FOX layer 12" (page 8 of Brief, last paragraph).

It is well settled that the presumption of validity attaching to the claims and supporting disclosure of a U.S. patent is substantial, and an applicant carries a heavy burden proving that a U.S. patent is inoperative or non-enabling. See In re Weber, 405 F.2d 1403, 1407, 160 USPQ 549, 553 (CCPA 1969);

[1] I.E.E.E. Electron Device Letters by Haddad; U.S. Patent 4,637,128; and Silicon Processing for the VLSI Era, Volume 2: Process Integration.

In re Spence, 261 F.2d 244, 246, 120 USPQ 82, 83 (CCPA 1958); In re Michalek, 162 F.2d 229, 231-32, 74 USPQ 107, 109 (CCPA 1947). In the present case, Yoo specifically claims forming the poly-silicon floating gate over a field oxide region. While appellant contends that the floating gate of Yoo is disclosed as "formed **over** a field oxide region, not specifically on a field oxide region" (page 8 of Brief, last paragraph), we agree with the examiner that when the patent claims are read in light of the accompanying illustrative drawings, it is proper to conclude that Yoo claims a polysilicon floating gate on, and in contact with, the field oxide region. Moreover, the presumption of validity and enablement of a U.S. patent attaches to unclaimed disclosures as well as claimed subject matter. Amgen, Inc. v. Hoechst Marion Roussel, Inc., 314 F.3d 1313, 1355, 65 USPQ2d 1385, 1416 (Fed. Cir. 2003).

As for the references cited by appellant, appellant has only demonstrated that in the specific environments discussed in the references, relatively thin gate oxides are employed. However, appellant has not established that one of ordinary skill in the art would not have interpreted the invention of Yoo, a particular device comprising a 4T SRAM and a floating gate memory on the

same integrated circuit, as comprising a polysilicon floating gate on a field oxide region, as called for in the appealed claims. The present record is devoid of the requisite objective evidence that the drawings of Yoo are in error.

In conclusion, based on the foregoing, the examiner's decision rejecting the appealed claims is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

EDWARD C. KIMLIN)
Administrative Patent Judge)
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BRADLEY R. GARRIS) BOARD OF PATENT
Administrative Patent Judge) APPEALS
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